REMARKS

The Examiner is thanked for the allowance of claims 1-18.

By the present amendments, Applicants have amended the specification to provide reference signs as shown in the drawings. Specifically, these reference signs, and related additional sentences, have been provided in light of the specification of U.S. Patent No. 6,114,753, issued September 5, 2000, which issued from Serial No. 08/857,674, filed May 16, 1997, of which the above-identified application is a Divisional application. It is respectfully submitted that these amendments to the specification, the subject matter thereof being in U.S. Patent No. 6,114,753, does not add new matter to the above-identified application.

The objection to the drawings under 37 CFR 1.83(a), on page 2 of the Office Action mailed January 14, 2002, is noted. In view thereof, Applicants are submitting concurrently herewith a Request for Approval of Drawing Amendments, including a new Fig. 9. In addition, the specification of the above-identified application has been amended in the Brief Description of the Drawings, to refer to this Fig. 9; and a paragraph has been added describing this Fig. 9. This Fig. 9 shows, inter alia, a three layer structure of the adhesive.

It is respectfully submitted that the concurrently filed new drawing Fig. 9, as well as the description in connection therewith in the present application, overcomes the drawing objection.

In view of the foregoing comments and amendments, entry of the present amendments, and passing of the above-identified application to issue in due course, are respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification by the current Amendment. This marked-up version is on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.35443VX1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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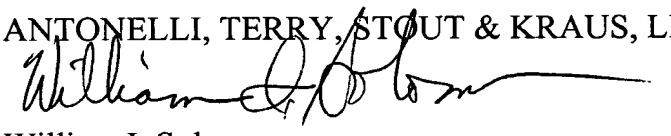

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE SPECIFICATION

Please add the following new paragraph on page 8, after line 1, as follows:

Fig. 9 shows a semiconductor device with a three layer structure for the adhesive layer. Shown is core layer (e.g., porous supporting layer) 10 with adhesive layers 20,20 on opposite sides of the core layer 10. Semiconductor chip 50 is provided on semiconductor supporting substrate 90. Lead 60, including wiring 40, is electrically connected to external connecting terminal 80 and electrode 100 of chip 50. Sealing material 70 covers lead 60.

Please delete the paragraph on page 8, lines 6-18, and substitute therefor the following new paragraph:

The process can be divided into three representative sections. The first one, including STEPS 1-5 (Fig. 2a), is a method for fabricating a semiconductor element comprising (1) the step 1 of applying an adhesive film 2.2 to the tape 2.1 having a pattern layer, (2) the step 2 of adhering the tape 2.1 having a pattern layer to the semiconductor element 2.3 by means of the adhesive film 2.2 while maintaining an insulating condition therebetween, (3) the step 3 of electrically connecting the pattern layer formed on the tape 2.1 and the pad 2.6 on the

semiconductor element 2.3, via connecting lead 2.1.1', formed from wire 2.1.1, (4) the step 4 of sealing the electrically connected portion with an insulating agent (e.g., mold resin) 2.4, and (5) the step 5 of forming an external terminal 2.5 on the tape for connection to the mounting substrate.

Please delete the paragraph bridging pages 8 and 9, and substitute therefor the following new paragraph:

The second one, including STEPS 6-10[,] (FIG. 2b), is a method for fabricating a semiconductor element comprising (1) the step 6 of applying an adhesive film 2.2 to the semiconductor element 2.3, (2) the step 7 of adhering the tape 2.1 having a pattern layer to the semiconductor element 2.3 by means of the adhesive film 2.2 while maintaining an insulating condition therebetween, (3) the step 8 of electrically connecting the pattern layer formed on the tape 2.1 and the pad 2.6 on the semiconductor element 2.3 via connecting lead 2.1.1', formed from wire 2.1.1, (4) the step 9 of sealing the electrically connected portion with an insulating agent 2.4, and (5) the step 10 of forming an external terminal 2.5 on the tape 2.1 for connection to the mounting substrate.

Please delete the paragraph on page 9, lines 12-23, and substitute therefor the following new paragraph:

The third one, including STEPS 11-14[,] (Fig. 2c), is a method of fabricating a semiconductor [clement] element comprising (1) the step 11 of setting the tape 2.1 having the pattern layer in registration and adhering the tape 2.1 to the semiconductor element 2.3 using the adhesive film 2.2 simultaneously with maintaining an insulating condition therebetween, (2) the step 12 of electrically connecting the pattern layer formed on the tape 2.1 and the pad 2.6 on the semiconductor element 2.3 via connecting lead 2.1.1', formed from wire 2.1.1, (3) the step 13 of sealing the electrically connected portion with an insulating agent 2.4, and (4) the step 14 of forming an external terminal 2.5 on the tape 2.1 for connection to the mounting substrate.

Please delete the paragraph bridging pages 10 and 11, and substitute therefor the following new paragraph:

As a general method for the above process, a method comprising the steps of transferring the tape, whereon the pattern is formed, by a long reel apparatus, stamping out the adhesive film into a designated shape, and adhering the adhesive film of the designated shape onto the circuit tape, as shown in Fig. 3, is

effective for mass production. Shown in FIG. 3 is reel 3.1 for the long circuit tape and reel 3.2 for the adhesive film. Punching jig 3.3, and adhesive film 3.4 on the circuit tape, are also shown in FIG. 3. When the adhesive film is made of a thermosetting resin, the adhesive film can be made to adhere to the circuit tape while in an uncured A stage or a half-cured B stage. The resin is then further cured to a condition of a final-cured C stage during the step of adhering the obtained circuit tape, to which the adhesive film is attached, to the semiconductor element. Otherwise, if the adhesive agent reaches the condition of the final cured C stage during the time that the adhesive film is adhered to the circuit tape, sometimes, an adhesive layer is newly formed on the cured film portion.

Please delete the paragraph bridging pages 11 and 12, and substitute therefor the new paragraph:

Fig. 4 shows an example of the composition of a circuit tape to which an adhesive film is attached. The circuit tape 4.1 can be adhered to the semiconductor element. If a thermosetting resin is used for the adhesive layer 4.2 at the circuit tape side and a thermoplastic resin is used for the adhesive layer 4.3 at the side adhered to the semiconductor, the circuit tape having the adhesive ability shown in Fig. 4 can be provided readily.

Please delete the paragraphs on page 18, lines 6-20, and substitute therefor the following new paragraphs:

The one is a peripheral pad arrangement as shown in Fig. 5. Fig. 5 shows semiconductor element 5.1 and pads 5.1.1. In this case, there are different types of structure for the arrangement of the external terminal of the semiconductor device, as shown in Figs. 6-1, 6-2, 6-3. That is, the case wherein the external terminals are located under the semiconductor element 6.3 (Fan In type, Fig. 6-1), the case wherein the external terminals are located outside the semiconductor element 6.3 (Fan Out type, Fig. 6-2), and the case wherein the external terminals are located at both under and outside the semiconductor element 6.3 (Fan In/Out type, Fig. 6-3) can be used.

Another example of the pad arrangement is the central arrangement shown in Fig. 7. Fig. 7 shows semiconductor element 5.1, and pads 5.1.1. In this case, the semiconductor device is composed of the structure shown in Fig. 8.

Please add the following new paragraph on page 20, after line 15, as follows:

Fig. 9 is a schematic cross section showing the structure of a

semiconductor device according to the present invention, having an adhesive film including a three layer structure.